REMARKS

Claims 1-20 are pending. Claims 1, 8 and 21 have been amended herein. Claims 1, 8 and 21 as amended are fully supported in the detailed description. No new matter has been added to the specification.

Double Patenting Rejection

Claims 1 and 8 are rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 12/005,745 in view of Chisholm et al., Winkler et al. and Wilcox. Copending Application No. 12/005,745 in view of Chisholm et al., Winkler et al. and Wilcox does not teach or suggest "a bypass register coupled to the bus master controller, wherein the bypass register has more than 8 bits is memory mapped and aggregates disk transaction information from memory mapped data transfers from a host CPU" as recited in Claim 1 (Claim 8 recites similar recitations). In the outstanding Office Action it is admitted that Application No. 12/005,745 does not teach the aforementioned limitation of Claims 1 and 8. However, it is alleged that Chisholm et al. teaches the aforementioned limitations of Claim 1. Applicants respectfully disagree. The shortcomings of Chisholm et al. with regard to these limitations are addressed below. The other relied upon references, Winkler et al. and Wilcox do not remedy the deficiencies of copending Application No. 12/005,745 and Chisholm et al. Accordingly, Applicants respectfully submit that copending Application No. 12/005,745 in view of Chisholm et al., Winkler et al. and Wilcox do not teach or suggest the embodiments set forth in Claims 1 and 8.

Section 35 U.S.C. 102 Rejection

Claims 1, 6, 8, 12 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicants' Admitted Prior Art (AAPA) in view of Chisholm et al., Winkler et al. and Wilcox. Applicants respectfully submit that the embodiments that are set forth in Claims 1, 6, 8, 12 and 21 are not rendered obvious by Applicants' Admitted Prior Art (AAPA) in view of Chisholm et al., Winkler et al. and Wilcox.

In particular AAPA in view of Chisholm et al., Winkler et al. and Wilcox does not teach or suggest "a bypass register coupled to the bus master controller, wherein the bypass register has more than 8 bits is memory mapped and aggregates disk transaction information from memory mapped data transfers from a host CPU" as recited in Claim 1. (Claims 8 and 15 recite similar recitations).

AAPA discusses an ADMA specification that is designed to improve ATA type devices. As discussed, the ADMA specification is designed to add features that improve the data transfer speed and efficiency of ATA devices. Moreover, AAPA discusses several of the shortcomings of ADMA that are not addressed in the prior art. It should be appreciated that AAPA does not discuss memory mapped data transfers such as is recited in Claim 1 (Claims 8 and 15 recite similar recitations).

As understood by Applicants, Chisholm et al. purportedly discloses an information handling system for transfer of command blocks to a local processing side without local processor intervention (see abstract). In the outstanding Office Action structures 203 and 311 are contended to teach the recited memory mapped bypass register (see page 18). More specifically, the transferring of command blocks using a command

block address provided to a register from CPU 103 is contended to teach the recited memory mapped bypass register. Applicants respectfully submit that the above described types of transfers are not memory mapped information transfers. A memory mapped information transfer is an information transfer that involves an address that is mapped to an address of the memory register. As indicated in the outstanding Office Action, Chisholm et al. discloses that command blocks are transferred using a command block address that is provided or generated by the CPU. However, the address that is provided by the CPU is not mapped to an address of the memory register. Accordingly, Chisholm et al does not teach or suggest a memory mapped register as is recited in Claims 1, 8 and 21.

The relied upon Winkler et al. and Wilcox references do not remedy the deficiencies of AAA and Chisholm et al. discussed above as regards the aforementioned limitations related to the recited memory mapped register. Accordingly, Applicants respectfully submit that AAA in view of Chisholm et al., Winkler et al. and Wilcox references do not teach or suggest the embodiment recited in Claims 1, 8 and 21.

CONCLUSION

Applicants respectfully assert that all claims are now in condition for allowance and Applicants earnestly solicit such action from the Examiner. The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

MURABITO, HAO & BARNES

Dated: 8-23-2010

/Reginald A. Ratliff/

Reginald A. Ratliff
Registration No. 48,098
Two North Market Street
Third Floor
San Jose, CA 95113
(408) 938-9060